WIRELESS LOCAL AREA NETWORK REPEATER WITH DETECTION

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is related to and claims priority from pending U.S. Provisional Application Number 60/426,541 filed November 15, 2002, and is further related to PCT Application PCT/US03/16208 entitled WIRELESS LOCAL AREA NETWORK REPEATER, the contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] The present invention relates generally to wireless local area networks (WLANs) and, particularly, the present invention relates to dynamic frequency detection in a frequency translating repeater.

[0003] Several standard protocols for wireless local area networks, commonly referred to as WLANs, are becoming popular. These include protocols such as 802.11 (as set forth in the 802.11 wireless standards), home RF, and Bluetooth. The standard wireless protocol with the most commercial success to date is the 802.11b protocol although next generation protocols, such as 802.11g, are also gaining popularity.

[0004] While the specifications of products utilizing the above standard wireless protocols commonly indicate data rates on the order of, for example, 11 MBPS and ranges on the order of, for example, 100 meters, these performance levels are rarely, if ever, realized. Performance shortcomings between actual and specified performance levels have many causes including attenuation of the radiation paths of RF signals, which for 802.11b are in the range of 2.4 GHz in an operating environment such as an

indoor environment. Access point to client ranges are generally less than the coverage range required in a typical home, and may be as little as 10 to 15 meters. Further, in structures having split floor plans, such as ranch style or two story homes, or those constructed of materials capable of attenuating RF signals, areas in which wireless coverage is needed may be physically separated by distances outside of the range of, for example, an 802.11 protocol based system. Attenuation problems may be exacerbated in the presence of interference in the operating band, such as interference from other 2.4GHz devices or wideband interference with in-band energy. Still further, data rates of devices operating using the above standard wireless protocols are dependent on signal strength. As distances in the area of coverage increase, wireless system performance typically decreases. Lastly, the structure of the protocols themselves may affect the operational range.

[0005] Repeaters are commonly used in the mobile wireless industry to increase the range of wireless systems. However, problems and complications arise in that system receivers and transmitters in any given device operate at the same frequency in a WLAN utilizing, for example, 802.11 WLAN or 802.16 WMAN wireless protocols. In such systems, when multiple transmitters operate simultaneously, as would be the case in repeater operation, difficulties arise. Typical WLAN protocols provide no defined receive and transmit periods and, thus, because random packets from each wireless network node are spontaneously generated and transmitted and are not temporally predictable, packet collisions may occur. Some remedies exist to address such difficulties, such as, for example, collision avoidance and random back-off protocols, which are used to avoid two or more nodes transmitting packets at the same

time. Under 802.11 standard protocol, for example, a distributed coordination function (DCF) may be used for collision avoidance.

[0006] Such operation is significantly different than the operation of many other cellular repeater systems, such as those systems based on IS-136, IS-95 or IS-2000 standards, where the receive and transmit bands are separated by a duplexing frequency offset. Frequency division duplexing (FDD) operation simplifies repeater operation since conflicts associated with repeater operation, such as those arising in situations where the receiver and transmitter channels are on the same frequency for both the uplink and the downlink, are not present.

[0007] Other cellular mobile systems separate receive and transmit channels by time rather than by frequency and further utilize scheduled times for specific uplink/downlink transmissions. Such operation is commonly referred to as time division duplexing (TDD). Repeaters for these systems are more easily built, as the transmission and reception times are well known and are broadcast by a base station. Receivers and transmitters for these systems may be isolated by any number of means including physical separation, antenna patterns, or polarization isolation. Even for these systems, the cost and complexity of a repeater may be greatly reduced by not offering the known timing information that is broadcast, thus allowing for more economically feasible repeaters. That being said, the techniques described herein may be combined with broadcast channel assignment information to aid the repeater in determining uplink and downlink timings, which may be required for centerally controlled TDD systems such as 802.20 or 802.16.

[0008] Thus, WLAN repeaters operating on the same frequencies have unique constraints due to the above spontaneous transmission capabilities and therefore require a unique solution. Since these repeaters use the same frequency for receive and transmit channels, some form of isolation must exist between the receive and transmit channels of the repeater. While some related systems such as, for example, CDMA systems used in wireless telephony, achieve channel isolation using sophisticated techniques such as directional antennas, physical separation of the receive and transmit antennas, or the like, such techniques are not practical for WLAN repeaters in many operating environments such as in the home where complicated hardware or lengthy cabling is not desirable or may be too costly.

[0009] One system, described in International Application No. PCT/US03/16208 and commonly owned by the assignee of the present application, resolves many of the above identified problems by providing a repeater which isolates receive and transmit channels using a frequency detection and translation method. The WLAN repeater described therein allows two WLAN units to communicate by translating packets associated with one device at a first frequency channel to a second frequency channel used by a second device. The direction associated with the translation or conversion, such as from the frequency associated with the first channel to the frequency associated with the second channel, or from the second channel to the first channel, depends upon a real time configuration of the repeater and the WLAN environment. The WLAN repeater may be configured to monitor both channels for transmissions and, when a transmission is detected, translate the received signal at the first frequency to the other channel, where it is transmitted at the second frequency.

[0010] The above described approach solves both the isolation issue and the spontaneous transmission problems as described above by monitoring and translating in response to packet transmissions and may further be implemented in a small inexpensive unit. However, a WLAN repeater in order to operate effectively must be capable of rapidly detecting the presence of a signal on one of at least two frequency channels used within the frequency translating repeater.

SUMMARY OF THE INVENTION

[0011] Accordingly, in various exemplary and alternative exemplary embodiments, the present invention extends the coverage area in a wireless environment such as a WLAN environment, and, broadly speaking, in any time division duplex system including IEEE 802.16, IEEE 802.20 and TDS-CDMA, with a dynamic frequency detection method. An exemplary WLAN frequency translating repeater allows two WLAN nodes or units to communicate by translating packets from a first frequency channel used by one device to a second frequency channel used by a second device. The direction of the conversion from channel 1 to channel 2, versus from channel 2 to channel 1, is dependent upon real time configuration. The repeater may preferably monitor both channels for transmissions, and when a transmission on a channel is detected, the repeater is configured to translate the received signal to the other channel, where it is transmitted.

[0012] In accordance with various exemplary embodiments, the presence of a signal on one of at least two channels must be detected with very little delay. Rapid signal detection can be difficult if processing is performed by an analog to digital converter (ADC) and a digital processor. Pipeline delays associated with the ADC and additional delays associated with the processor create obstacles to rapid detection.

[0013] RF in circuit propagation delays may be used to facilitate rapid detection by allowing analog storage of received waveforms while signal detection and transmitter configuration take place. Signal detection may be performed prior to the expiration of RF delay periods, thereby providing additional time to perform the required configuration for the system.

[0014] Detection of received waveforms is preferably accomplished using logarithmic amplifiers (log amps) as will be described in greater detail herein after. Outputs from log amps are fed to an ADC and then to a processor. As will be appreciated, the delay associated with such an architecture drives the cost and performance of an exemplary repeater. One benefit of using an ADC in connection with a processor is the ability to convert analog signals and the ability to add additional intelligence to the detection process, but at the cost of additional delay and expense. Thus, an alternative to such an architecture is an architecture whereby fast analog detectors work in connection with a supervisory processor which can override decisions made by fast analog detection portions.

[0015] RF delays are preferably implemented using Surface Acoustic Wave (SAW) filters. SAW filters provide the capability to enable analog signal storage, to provide channel selection, to provide jammer suppression, to provide a "feed-forward" variable gain control path, and the like. An exemplary detection process in accordance with various exemplary embodiments may be performed in an analog only configuration using a threshold comparator. It will be appreciated that such an analog only mode would not make use of an ADC directly. An exemplary processor may play a role in the detection process to, for example, actively control the analog reference voltage associated with detection comparators used to make the detection decisions. Alternatively, the output of the log amps may be digitized and the detection decision may be made in an all digital fashion. As noted above, a draw back of an all-digital architecture is that high speed ADCs and a high performance processor are required leading to relatively high expenses. An additional problem

associated with the use of an all digital path and a processor is the significant delay associated with digital sampling and decision making.

[0016] In accordance with various exemplary embodiments, an analog comparator may be used having a processor-controlled threshold. The exemplary analog comparator may further be equipped with a digital override to allow a fast initial decision to be made based on analog detection, while providing a slower more accurate and controllable final decision to be made using the processor. For example, when a signal from an interferer is detected, and the processor recognizes that the packet duration is longer than the wireless protocol will allow, the AGC and/or the detector may be forced by the processor to turn off the output signal transmission. It will be appreciated that the AGC gain setting may be directly controlled and overridden providing usefulness in situations including detection of system feed-back oscillations, detection or occurrence of a false alarm, detection of interference, expiration of valid packet intervals and the like.

[0017] The use of analog detection and initial control allows for low latency detection and system configuration, while the use of a processor allows the additional robust control. Algorithms for achieving control may include characterization and assessment of interference from different devices, establishment of initial system configuration, decoding of potential repeater control commands, the determination of system oscillations, and the like.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The accompanying figures, where like reference numerals refer to identical or functionally similar elements throughout the separate views and which together with the detailed description below are incorporated in and form part of the specification, serve to further illustrate various embodiments and to explain various principles and advantages in accordance with the present invention

[0019] FIG. 1 is a diagram illustrating a WLAN including an exemplary repeater having automatic gain control in accordance with various exemplary embodiments.

[0020] FIG. 2 is a schematic drawing illustrating an exemplary gain control circuit associated with an exemplary repeater of FIG. 1.

[0021] FIG. 3 is a schematic drawing illustrating an exemplary detector circuit associated with an exemplary repeater of FIG. 1 and FIG. 2.

[0022] FIG. 4 is a flow chart illustrating an exemplary detection procedure associated with various embodiments of an exemplary repeater.

DETAILED DESCRIPTION OF THE INVENTION

[0023] Referring now to FIG. 1, a wide area connection 101, which could be, for example, an Ethernet connection, a T1 line, a wideband wireless connection or any other electrical connection providing a data communications path, may be connected to a wireless gateway, or access point (AP) 100. The wireless gateway 100 sends RF signals, such as IEEE 802.11 packets or signals based upon Bluetooth, Hyperlan, or other wireless communication protocols, to client units 104, 105, which may be personal computers, personal digital assistants, or any other devices capable of communicating with other like devices through one of the above mentioned wireless protocols. Respective propagation, or RF, paths to each of the client units 104, 105 are shown as 102, 103.

[0024] While the signal carried over RF path 102 is of sufficient strength to maintain high-speed data packet communications between the client unit 104 and the wireless gateway 100, the signals carried over the RF path 103 and intended for the client unit 105 would be attenuated when passing through a structural barrier such as walls 106 or 107 to a point where few, if any, data packets are received in either direction if not for a wireless repeater 200, the structure and operation of which will now be described.

[0025] To enhance the coverage and/or communication data rate to the client unit 105, wireless repeater 200 receives packets transmitted on a first frequency channel 201 from the wireless gateway 100. The wireless repeater 200, which may be housed in an enclosure typically having dimensions of, for example, 2.5"x3.5"x.5", and which preferably is capable of being plugged into a standard electrical outlet and

operating on 110 V AC power, detects the presence of a packet on the first frequency channel 201, receives the packet and re-transmits the packet with more power on a second frequency channel 202. Unlike conventional WLAN operating protocols, the client unit 105 operates on the second frequency channel, even though the wireless gateway 100 operates on the first frequency channel. To perform the return packet operation, the wireless repeater 200 detects the presence of a transmitted packet on the second frequency channel 202 from the client unit 105, receives the packet on the second frequency channel 202, and re-transmits the packet on the first frequency channel 201. The wireless gateway 100 then receives the packet on the first frequency channel 201. In this way, the wireless repeater 200 is capable of simultaneously receiving and transmitting signals as well as extending the coverage and performance of the wireless gateway 100 to the client unit 105.

[0026] To address the difficulties posed by obstructions as described above and attendant attenuation of the signal strength along obstructed paths and thus to enhance the coverage and/or communication data rate to client unit 105, exemplary wireless repeater 200, as shown in FIG. 1, may be used to retransmit packets beyond a range limited by propagation path constraints through, for example, frequency translation. Packets transmitted on a first frequency channel 201 from AP 100 are received at repeater 200 and re-transmitted, preferably with a greater power level, on a second frequency channel 202. Client unit 105 preferably operates on second frequency channel 202 as if AP 100 were also operating on it, such as with no knowledge that AP 100 is really operating on first frequency channel 201 such that the frequency translation is transparent. To perform return packet operations, repeater unit 200 detects the presence of a transmitted return packet on second frequency channel 202

from client unit 105, and is preferably configured to receive the packet on second frequency channel 202, and to retransmit the data packet to, for example AP 100, on first frequency channel 201.

[0027] Wireless repeater 200 is preferably capable of receiving two different frequencies simultaneously, such as first frequency channel 201 and second frequency channel 202 determining which channel is carrying a signal associated with, for example, the transmission of a packet, translating from the original frequency channel to an alternative frequency channel and retransmitting the frequency translated version of the received signal on the alternative channel. Details of internal repeater operation may be found in co-pending PCT Application No. PCT/US03/16208.

[0028] Repeater 200 may thus receive and transmit packets at the same time on different frequency channels thereby extending the coverage and performance of the connection between AP 100 and client unit 105, and between peer-to-peer connections such as from one client unit to another client unit. When many units are isolated from one another, repeater unit 200 further acts as a wireless bridge allowing two different groups of units to communicate where optimum RF propagation and coverage or, in many cases, any RF propagation and coverage was not previously possible.

[0029] In accordance with various exemplary embodiments, repeater 200 is preferably configured to receive a signal and translate the frequency of the received signal with very little distortion or loss of the signal by properly controlling the gain of an exemplary transceiver section via Automatic Gain Control (AGC) circuitry (301

- 306) shown, for example, in FIG. 2. In a preferred embodiment, wireless repeater 200 shown is capable of receiving two different frequencies simultaneously, determining which one is present, translating the frequency of the one that is present to the other frequency and retransmitting a frequency translated version of the received signal.

[0030] In accordance with one preferred exemplary embodiment, AGC circuitry (301 - 306) utilizes RF delay and filter elements 307-310 to allow analog storage of an exemplary received waveform while signal detection and transmitter configuration takes place. It should be noted that signal detection may occur both prior to and during transit of signals in RF delay elements 307-310 providing time to perform system configuration. It should be noted that a detector power level is preferably used to set a gain value on a parallel signal path as part of the gain control operation.

[0031] More specifically, the AGC circuitry includes logarithmic amplifiers 301 and 302, AGC control circuits 303 and 304, gain control elements 305 and 306, which may preferably include variable gain or variable attenuator elements, and RF delay elements 307-310 which may preferably include analog storage devices such as, for example, delay lines and/or band pass filters. Low pass filter 311 and 312, and analog to digital converter (ADC) 313 and 314 are further preferably used to accomplish gain control under the direction and control of, for example, processor 315.

[0032] Since repeater 200 is configured to simultaneously detect and process two different frequency signals, received signal 330 is split and propagated on two different RF paths, for example, using RF splitter 316. Likewise, because the two

different frequency paths must be delayed and controlled separately, each signal path is further split by, for example, IF splitters 317 and 318. One of the split signal outputs from IF splitter 317 is preferably coupled to logarithmic amplifiers 301 and the other split signal output is preferably coupled to gain control elements 305. Likewise, one of the split signal outputs from IF splitter 318 is preferably coupled to logarithmic amplifiers 302 and the other split signal output is preferably coupled to gain control elements 306. The output of logarithmic amplifiers 301 is fed to AGC control circuit 303 and low pass filter 311. Likewise, the output of logarithmic amplifiers 302 is fed to AGC control circuit 304 and low pass filter 312. It should be noted that while logarithmic amplifiers 301 and 302 preferably provide an output voltage proportional to the logarithm of the power of received signal 330, tracking the envelope thereof, other devices known to those of ordinary skill in the art may also be used to track the envelope or samples of the envelope directly or proportionately.

[0033] The basic operation of components along the detection path of received signal 330 such as, for example, low pass filters 311 and 312, analog-to-digital converters (ADC) 313 and 314, and processor 315 for example, would be readily apparent to those of ordinary skill in the art and thus a detailed review of the basic operation thereof is omitted, such operation is disclosed in detail in commonly assigned co-pending PCT Patent Application No. PCT/US03/16208. However it should be briefly noted that processor 315 preferably detects the presence of an IF signal on detection paths DET1 331 and DET2 332. As described in the above identified co-pending application, signal detection may be based on the signal level exceeding a threshold using, for example, analog or digital signal comparison implements in processor 315, or could be performed by other means well known to

those of ordinary skill in the art. Once the signal is detected, gain control is applied to the signal using for example, AGC control circuits 303 and 304 on IF path IF1 333 or IF2 334 respectively, depending on the channel.

[0034] With reference still to FIG. 2 of the drawings, gain control is applied to signals on IF paths IF1 333 and IF2 334 using AGC control circuits 303 and 304 which circuits provide, *inter alia*, filtering of the analog voltage at the output of, for example, logarithmic amplifiers 301 and 302, any DC offset adjustment which may be necessary, AGC set point reference and control, level shifting/scaling, any required polarity reversal, and the like as would be appreciated by one of ordinary skill in the art. The output of AGC control circuits 303 and 304 are fed to gain control elements 305 and 306 which may provide either adjustable gain or adjustable attenuation of received signal 330 based on a value associated with, for example, the desired transmitter output power. It should be noted that AGC control circuits 303 and 304 may be one of a variety of gain control circuits, devices, or the like, as would be well known to those of ordinary skill in the art.

[0035] As an example of gain control in accordance with various exemplary embodiments, a variable attenuator could be used for gain control element 305 under the following conditions: desired output power +15dBm, received signal power -80dBm, total transceiver losses 65dB, total transceiver gains 165dB.

[0036] Under these conditions, a variable attenuator associated with, for example, gain control element 305, should be set according to the relation: Rx Signal Power - Desired Output Power + Total Gains - Total Losses, thus the attenuation would be -

80dBm – 15dBm +165dB – 65dB resulting in 5dB of attenuation. It will be appreciated that a voltage may be calculated and applied to the gain control element 305, for example, by AGC control circuit 303 resulting in the desired 5dB attenuation setting. It should also be noted that while ACG control circuit 303 and gain control element 305 are described herein, the above description applies to the operation of AGC control circuit 304 and gain control element 306.

[0037] Thus, receive signal 330 in order to be retransmitted in accordance with various exemplary embodiments, and in accordance with the present example, is preferably output from gain control element 305 and delayed via Surface Acoustic Wave (SAW) filters 308 and 310. It will be appreciated that the delay introduced by SAW filters 308 and 310 acts to essentially store the analog waveform while AGC and signal detection processes, for example as described above, are carried out, meaning that detection and gain control setting are preferably completed during the propagation interval of the signal.

[0038] In accordance with various exemplary and preferred exemplary embodiments, RF delays are imposed through SAW filters 307-310 enabling analog signal storage and channel selection, jammer suppression, and a feed-forward variable gain control path. AGC control circuits 303 and 304 and gain control elements 305 and 306 may be biased or otherwise set under control of for example processor 315, which is preferably a processor, such as a general purpose processor, dedicated processor, signal processing processor, or the like as would be understood by one of ordinary skill in the art. Further, set points may be obtained by processor 315 from a look up table or the like depending on which channel received signal 330 is received

on and which channel is selected for signal retransmission. It should be noted that different bands have different transmit power limitations in different countries, thus the selection of gain set points may be driven by several factors resulting from the need to meet FCC requirements and related specifications for the desired band such as spectral re-growth and Effective Isotropic Radiated Power (EIRP).

[0039] After detection and setting of the gain control, IF switch 319 and LO switch 320 are preferably set to retransmit received signal 330 at a different frequency without significantly cutting off the waveform preamble. It is important to note that detection and power sensing, for example, as described above, is preferably performed on detector paths DET1 331 and DET2 332, but actual gain control may be applied the on IF paths IF1 333 and IF2 334. More specifically referring again to FIG. 2, outputs from the logarithmic amplifiers 301 and 302 are fed to AGC control circuits 303 and 304 which circuits are making adjustments either as variable gain or attenuation with regard to gain control elements 305 and 306.

[0040] One factor in determining a sequence of signal detection and gain control is the effect caused by splitting the output voltage from logarithmic amplifiers 301 and 302 into a signal detection path and a gain control path, each having potentially two different filter bandwidths. As can be noted from FIG. 2, the gain control path is the path to AGC control circuits 303 and 304, while the signal detection path is the path leading to low pass filters 311 and 312, as previously described. Thus, if desired, the AGC control values and the signal detection filter bandwidth could be set differently. For example, the AGC control loop could be set to react very quickly to the incoming power envelop while signal detection, as carried out, for example, in ADC 313 and

314 and processor 315, could be configured to react more slowly. As a result, received signal 330 propagating in gain control elements 305 and 306 can be tracked very accurately while the portion of received signal 330 propagating in ADC 313 and 314 and processor 315 may track more slowly, but with more detection process gain.

[0041] It should be noted that in accordance with various exemplary and preferred exemplary embodiments, two separate detectors are used for performing detection of the presence of received signal 330 and for detection of the power level thereof in order to set gain. Thus, since signal detection may occur more slowly than AGC as described, different signal detection and AGC filter bandwidths may be used beneficially, allowing variable control elements associated with AGC such as gain control elements 305 and 306 to have a faster or slower response than the output of filters 311 and 312.

[0042] Another factor in controlling gain is the relative distance between the receive and transmit channels. Specifically, depending on the distance therebetween, the target output power or set point from the gain control elements 305 and 306 can be different to the extent that additional performance may be gained when the receive and transmit channels are further apart in frequency. Gain values may be increased in gain control elements 305 and 306 while continuing to meet performance requirements. Further, AGC control circuits 303 and 304 may be programmed to increase power based on the frequency difference or, alternatively, processor 315 may be programmed to control AGC control circuits 303 and 304 based on frequency separation. Adjusting set points based on frequency separation may further include

applying more filtering to any leakage signals picked up by a receiver to avoid self interference.

[0043] A factor affecting the choice of which channels to operate on during initial repeater power up may be influenced by choosing repeating channels based on the ability to transmit more power in different FCC bands or bands controlled by other regulatory bodies. For example, in the U-NII bands for operation in the United States, the maximum allowable transmit power for CH36-48 is 50mW, for CH52-64 is 250mW, and for CH149 – 161 is 1W. Therefore it is possible to receive a signal in on a channel associated with one of the lower power bands and choose a channel on a different band allowing higher transmit power, thereby allowing a higher AGC set point. Thus the set points for a translation, say from F1 to F2 and F2 to F1 would be different. The decision of which channels to select is preferably pre-programmed during manufacturing, or, alternatively could be programmed in the field, in, for example, AGC control circuits 303 and 304 or processor 315.

[0044] In accordance with other aspects of the present invention, gain control may require AGC calibration during initial manufacturing. Calibration may be desirable to allow the use of lower tolerance parts thus reducing cost. Calibration may further provide for accuracy required for regional or band specific power settings. Accordingly, calibration may include setting up circuits and devices in accordance with one or more of the following; regional regulatory rules, frequency channel, received power level, transmit power level, temperature, and the like. In accordance with various exemplary and preferred exemplary embodiments, repeater 200 using, for example, processor 315, may store calibration tables and the like and be

configured, for example through the use of software, programs, instructions or the like, to pass specific calibration values to AGC control circuits 305 and 306. Processor 315 would preferably utilize a digital to analog conversion process to control the set point.

[0045] As mentioned above, different detector outputs may be used for AGC and signal detection. Signal detection may be performed in an analog only configuration using, for example, a threshold comparator under the control of processor 315 which may be configured to actively control, for example, an analog reference voltage a threshold comparator uses to make the detection decision. Alternatively, received signal 330 may be digitized and a detection decision made, for example, in processor 315. One concern related to using a digital path and processor 315 includes delay associated with, for example, digital sampling and decision-making instructions in a processor 315.

[0046] In accordance with various alternative exemplary embodiments an analog comparator (not shown) having a threshold controlled by processor 315 may be used. Such a configuration could be equipped with a digital override to allow for a fast initial decision, converging to a slower more accurate and controllable decision using software, programs, instructions, and the like readable and executable by processor 315. For example, if an interferer is detected, and processor 315 recognizes that the packet duration is longer than the wireless protocol will allow, AGC control circuits 303 and 304 and/or detector could be turned off by processor 315 to prevent signal transmission. Thus the normal AGC setting may be directly controlled and

overridden. Such control is further useful in situations including when a system feedback oscillation is detected.

[0047] In addition to AGC control, and detection as illustrated and described with reference FIG. 2, an alternative to detector processing block is depicted in FIG. 3. It will be appreciated that inputs 400 and 401 are preferably coupled with the outputs of filter 311 and filter 312 replacing ADC 313 or 314 and, at least for detection purposes, processor 315. It should be noted that while the exemplary detection circuit shown in FIG. 3 is indicated to replace processor 315 for purposes of performing digital detection, processor 315 in accordance with various exemplary embodiments remains present in frequency translating repeater 200 for performing other functions as will be described herein. It will further be appreciated that the exemplary circuit illustrated in FIG 3 may be replicated twice, once for each of the detector paths leading from 313 and 314.

[0048] Thus, inputs 400 and 410 are preferably coupled to threshold comparators 401 and 411 respectively. The reference threshold of comparators 401 and 411 is preferably set by digital to analog converters (DAC) 404 and 414 which may be internal to the processor 315 or may be provided externally, and may further be simple pulse width modulators or pulse density modulators. DAC 404 and DAC 414 are preferably controlled by processor 315 and are preferably programmed based upon factors such as, for example, a probability of detection and a probability of false detection as derived by various algorithms known to those of ordinary skill in the art.

[0049] It will be appreciated that detection algorithms may be based on a statistical analysis of samples of a received signal at ADCs 402 and 412 and can include level crossing rates, average multipliers, and the like. Alternatively a SAW tooth control algorithm may be used to observe the "qualified" false detection rate, for example, on comparator 401 and 411. The SAW tooth control algorithm works by determining when a false detection has occurred and further qualifying the false detection using known parameters of the relevant packet protocol, such as packet duration and the like. If a threshold is crossed for only short periods of time, shorter than the packet duration, a false detection is most probable. It should be noted that valid ranges for packet durations are defined in accordance with protocol standards and specifications, such as 802.11 and the like. If a detection interval is too short, the detection cannot be associated with a valid 802.11 packet. If a detection interval is too long, the detection cannot be associated with a valid 802.11 packet either.

[0050] Accordingly, it would be likely that in such situations, the detection threshold is set too low, interference may be present, the repeater could be oscillating, or the like. A SAW tooth control algorithm adds an increment to the threshold for the comparator every time a false detection occurs, then subtracts a small amount from the threshold every time there is no detection. It will be appreciated that the relative increments and decrements of the detection threshold level will determine the false alarm rate, and the time constant of the resulting control loop. While SAW tooth control schemes have been effectively used in reverse link "outer loop power control" in, for example, IS-95 CDMA base stations, the application of a SAW tooth control loop to detection in accordance with various exemplary embodiments, provides advantages not previously appreciated.

[0051] Once reliable detection thresholds are set, two control lines may be output in connection with the "fast detect" analog circuitry. Channel A/Channel B line is preferably output from OR element 407 for controlling switches in FIG 3 which determine which IF channel is up-converted and transmitted. The other control line PA_ON is preferably output from AND element 417, and may be used to enable, disable, or otherwise control the output of the transmitter by enabling or disabling the power amplifier. It should be noted that OR element 407 and AND element 417 are provided to allow processor 315 a final degree of control over the respective outputs through override signals. Actual generation of logic levels associated with detection is preferably performed by AND element 406 and OR element 416. For PA control, outputs of comparators 401 and 411 are input to OR function 416.

[0052] For Channel A and Channel B detection, output signal 415 from comparator 411 is coupled to into an inverting input of AND element 406 resulting in an input which is "active low" and will produce a logic 0 on the output of AND element 406 when a signal is present on channel B. When a signal is present on channel A, output signal 405 from comparator 401 will be active and preferably a logic 1 or high level, producing a logic 1 or high level on the output of AND 406 provided that input "Override 1" is present. Override 1 signal preferably allows the processor to directly control the A/B line despite the presence or absence of signals. For example, if Override 1 is set low, the output will be forced to a low output indicative of channel B detection. If Override 1 is set high, AND element 406 will operate normally. To force the selection of Channel A, processor 315 preferably activates Override 2 which is input to OR element 407 forcing the output high indicative of channel A detection.

[0053] It will be appreciated that the functioning of the PA_ON may be controlled by processor 315. Override 3 signal can be set to force the PA_ON into the high or ON position. OR element 416 provides a high or ON output for PA_ON when a signal is detected and an output generated on either comparator 401 or 411. AND element 417 provides a mechanism in connection with Override 4 signal, for processor 315 to force PA_ON into an off, or disabled state. Processor 315 may further force PA_ON into an on state even when no signal is present through the use of Override 3. It will be appreciated that while the above described override and enabling functions are preferably provided by AND elements 406 and 417 and OR elements 416 and 407, they may be implemented in other ways. For example, the Channel A/Channel B line may generated as an analog comparator output with inputs connected to analog detectors outputs 400 and 410, and the PA_ON signal may be generated as a combination of detector outputs 400 and 410 and a single threshold detector.

[0054] It should be noted that the above description represent one example demonstrating various control functions capable of facilitating the integration of a fast fixed analog detection and a slow more intelligent digital detection. A flowchart is shown in FIG. 4, depicting an exemplary control algorithm which may preferably be implemented in the processor 315 in FIG. 2. Upon power-up processor 315 begins operation at 500, performing various initial system configuration tasks in 501. It will be appreciated that start-up tasks could include power-on self-tests, initial channel selection, and repeater calibrations. Next, flow passes to normal operation with decision 502. If no signal is present on either of the detectors, processor 315 will

monitor the detectors and refine the threshold settings. It should be noted that there are two preferable approaches to refining detection and thresholding algorithms. First, if processor 315 uses ADCs to monitor detector signals, a statistical analysis may be performed to set the threshold directly. If the comparator output only is monitored, qualified false detection may be used in accordance with the above described saw tooth algorithm. A combination of saw tooth algorithms may further be used to improve the quality of detection. For example, a saw tooth based on false alarm rates may be combined with a faster statistical approach associated with a short-term level adjustment based on a direct measurement. It should be noted that with direct measurement techniques, a sampling rate associated with the ADCs is not required to meet conventional Nyquist criteria required to reconstruct a signal. Instead, since samples are being used only for statistical analysis, a significantly lower sampling rate may be used allowing low cost processors to be used, including integrated low speed ADCs.

[0055] As thresholds associated with comparators 401 and 411 are refined and set by processor 315, first in initial system configuration 501 and then refined for example, at 503, signal detection continues at 502. When a signal is detected, a post qualification is preferably performed in one of several ways at 504. One technique involves monitoring the output of comparators 401 and 411 for a predetermined duration, such as an expected packet interval, to ensure valid detection continues to be present. Another technique may involve sampling the comparator input, for example using ADC 402 and 412, and determining how far above the threshold the signal is providing a further level of confidence that the initial detection is not a false alarm. During detection at 502, one of comparators 401 and 411 havealready been

configured to begin transmission of the information contained in the signal, such as a packet, independent of processor 315. Post qualification at 504, thus ensures that no mistake in detection has been made, and to provide a corrective mechanism if one has. While digital processing is slower than fast analog detection, it is less prone to system noise. Therefore, once a detected signal is post qualified, control of the transmitter will be taken away from analog circuits and overridden by processor 315 providing faster transmitter turn on, and robust detection which is less sensitive to signal detection anomalies. Further, since transmitter turn off is not as time critical as transmitter turn on, it can be performed by processor 315 alone. If post qualification testing determines that the detection was a false alarm at 505 the transmitter is preferably turned off at 506, and the false alarm will be logged. It should be noted that information obtained from the logging of false alarms may be used, for example, by processor 315 to cause a change in the threshold, in accordance with the saw tooth algorithm described herein above. Alternatively, logged information may be used for performance analysis.

[0056] If detection is valid and not determined to be a false alarm, a packet timer may be started and a digital override of the transmitter performed at 507 to "lock" it on, providing a reduction of sensitivity to noise in a low signal strength environment. The packet timer will be useful to determine if the duration of the received transmission is within reasonable and valid time limits within the scope of various standards, like 802.11, wherein packets have a specified minimum and a maximum duration in time. It will be appreciated that packet duration time limits may be used to qualify a received transmission to determine if a packet duration is valid or invalid. If the packet duration as determined by the packet timer is too short, the detected signal was either a random false detection caused by noise or the like, RADAR, or

other interference as will be appreciated by those of ordinary skill. If the packet duration as determined by the packet timer is too long, the detected signal may be associated with interference such as would be caused by a cordless phone, microwave, or the like, or may be caused by an oscillation condition due, for example, to self-oscillation within the same repeater, or may be associated with a system oscillation as would result from two repeaters operating within range of each other. Thus, the timer is tested at 508 to determine if the minimum packet duration has elapsed. If not, and the signal continues to be present, false alarm criteria may be refined at 509 and the condition re-tested at 511, whereupon the timer may continue to be monitored at 508, criteria refined at 509, and false alarm condition re-tested at 511. If a false alarm due to early termination is detected, for example based on the signal no longer being present, as false alarm is logged and transmitter disabled at 506. If the minimum packet duration as measured by the timer has been exceeded in accordance with, for example, 802.11 or appropriate protocol at 508, new criteria for determining the occurrence of a valid end of packet may be refined at 510. If the timer indicates that the duration of signal detection has not exceeded the maximum possible packet duration at 512, end of packet criteria at 510 are used at 514 to determine if the packet has terminated. If not, criteria are further refined at 510 and timer re-tested at 512. If the end of packed it detected at 514, the transmitter is turned off and the signal detection process is started again at 502. If the timer exceeds the maximum packet duration, and signal continues to be present, the transmitter is turned off at 513.

[0057] Detectors are preferably monitored at 515 to determine if detection ceases. If so, it can be assumed that the detected signal was likely due to a system oscillation or a self-jamming condition at 517 and in which case repeater is preferably reconfigured and detection restarted at 501. If detection does not cease indicating that

the signal has not dropped, then it can be assumed that the detected signal is likely an interferer, and the threshold is preferably modified at 516 to prevent the detection of interference, whereupon processor 315 preferably returns to normal detection at 502. It should be noted that in accordance with 802.11h, a requirement for detect RADAR is specified. Post analysis of the false detection conditions to characterize RADAR interferers may be incorporated in accordance with various exemplary embodiments. It will be appreciated that RADAR signals due to certain well-defined pulse durations and repetition profiles and the like may be easily characterized and false alarms associated with RADAR easily detected, for example, in post-qualification at 504.

[0058] One of ordinary skill in the art will recognize that as noted above, various techniques can be used to determine different signal detector configurations and set detection thresholds and the like in the present invention. Additionally, various components, such as detector elements 401 and 411, logic elements 406, 407, 416, and 417, DACs 404, 414, ADCs 402, 412 and the functionality of processor 315 and other elements could be combined into a single integrated device. Other changes and alterations to specific components, and the interconnections thereof, can be made by one of ordinary skill in the art without deviating from the scope and spirit of the present invention.